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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,587	03/29/2004	Reed W. Adams	TI-37110	2090

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,587	ADAMS ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6 and 15-20 rejected under 35 U.S.C. 102(b) as being anticipate by Kureya et al. (JP 2003-283318).

As to claim 1, Kureya et al. discloses in figure 1 an arrangement for generating a power up clear (PUC) signal based on a value of a supply voltage (Vdd), the arrangement comprising: a first circuit element (N1) of a first conductivity type (N type) having a first characteristic threshold voltage; a second circuit element (P2) of a second conductivity type (P type) having a second characteristic threshold voltage; a first circuit (1), including the first circuit element, configured to provide a first comparison input signal; a second circuit (2), including the second circuit element, configured to provide a second comparison input signal; and a comparator (CMP) for comparing the first and second comparison input signals, to cause the PUC signal to transition to an active state when one of the first and second comparison signals crosses another of the first and second comparison signals in response to an increasing magnitude of the supply voltage.

As to claim 2, figure 1 shows that the comparator determines the PUC signal based only on the first and second comparison input signals, without reference to any externally supplied reference voltages or currents or bias voltages or currents.

As to claim 3, figure 1 shows that the first characteristic threshold voltage is an n-channel MOSFET threshold voltage.

As to claim 4, figure 1 shows that the first circuit includes: an n-channel MOSFET (N1); and a resistance (R1), operative with the n-channel MOSFET so as to provide the first comparison signal to the comparator.

As to claim 5, figure 1 shows that the first circuit is configured to provide the first comparison signal that is substantially constant (equal to the threshold of transistor N1) after the supply voltage exceeds the n-channel MOSFET threshold voltage.

As to claim 6, figure 1 shows that the second characteristic threshold voltage is a p-channel MOSFET threshold voltage.

9. (Original) An arrangement of Claim 1, further comprising:

a hysteresis arrangement, configured to ensure that, after the comparator causes the PUC siral to transition to an active state in response to the supply voltage exceeding a first level, the PUC siral remains in the active state for so long as the supply voltage continues to exceed a second level that is a non-zero voltage margin smaller than the first level.

10. (Original) The arrangement of Claim 9, wherein the hysteresis arrangement includes:

a switch element, configured to adjust at least one of the first and second comparison sigizals.

As to claims 15 and 20, figure 1 shows a method, and a system thereof, for generating a power up clear (PUC) signal based on a value of a supply voltage, the method comprising: providing a first comparison input signal (at node a) that is based on a first characteristic threshold voltage of a first circuit element (N1) of a first conductivity type; providing a second comparison input signal (at node b) that is based on a second characteristic threshold voltage of a second circuit element (P2) of a second conductivity type; and comparing (by CMP) the first and second comparison input signals, to cause the PUC signal to transition to an active state when one of the first and second comparison signals crosses another of the first and second comparison signals in response to an increasing magnitude of the supply voltage.

As to claim 16, figure 1 shows the step of determining the PUC signal based only on the first and second characteristic threshold voltages, without reference to any externally supplied reference voltages or currents or bias voltages or currents.

As to claim 17, figure 1 shows that the first characteristic threshold voltage is an n-channel MOSFET threshold voltage.

As to claim 18, figure 1 shows that the second characteristic threshold voltage is a p-channel MOSFET threshold voltage.

As to claim 19, figure 1 shows that the comparing step constitutes: determining the PUC signal based only on an n-channel MOSFET threshold voltage constituting the first characteristic threshold voltage, and a p-channel MOSFET threshold voltage constituting the second characteristic threshold voltage, without reference to any externally supplied reference voltages or currents or bias voltages or currents.

3. Claims 1-4 and 5-20 rejected under 35 U.S.C. 102(e) as being anticipate by Olsen (US 20040201404).

As to claim 1, Olsen discloses in figure 3 an arrangement for generating a power up clear (PUC) signal based on a value of a supply voltage (Vdd), the arrangement comprising: a first circuit element (M2) of a first conductivity type (N type) having a first characteristic threshold voltage; a second circuit element (M31) of a second conductivity type (P type) having a second characteristic threshold voltage; a first circuit (105), including the first circuit element, configured to provide a first comparison input signal; a second circuit (110), including the second circuit element, configured to provide a second comparison input signal; and a comparator (115, 120, 125) for comparing the first and second comparison input signals, to cause the PUC signal to transition to an active state when one of the first and second comparison signals crosses another of the first and second comparison signals in response to an increasing magnitude of the supply voltage.

As to claim 2, figure 3 shows that the comparator determines the PUC signal based only on the first and second comparison input signals, without reference to any externally supplied reference voltages or currents or bias voltages or currents.

As to claim 3, figure 3 shows that the first characteristic threshold voltage is an n-channel MOSFET threshold voltage.

As to claim 4, figure 3 shows that the first circuit includes: an n-channel MOSFET (M2); and a resistance (M6, M9), operative with the n-channel MOSFET so as to provide the first comparison signal to the comparator.

As to claim 6, figure 3 shows that the second characteristic threshold voltage is a p-channel MOSFET threshold voltage.

As to claim 7, figure 3 shows that the second circuit includes: a p-channel MOSFET (M31); and a resistance ladder (M29, M30), operative with the p-channel MOSFET so as to provide the second comparison signal to the comparator.

As to claim 8, figure 3 shows that the second circuit is configured to provide the second comparison signal to that varies as a function of the supply voltage and crosses the first comparison signal when the supply voltage has increased to a value exceeding a sum of the first and second characteristic threshold voltages.

As to claim 9, figure 3 shows a hysteresis arrangement (140), configured to ensure that, after the comparator causes the PUC signal to transition to an active state in response to the supply voltage exceeding a first level, the PUC signal remains in the active state for so long as the supply voltage continues to exceed a second level that is a non-zero voltage margin smaller than the first level.

As to claim 10, figure 3 shows that the hysteresis arrangement includes: a switch element (140), configured to adjust at least one of the first and second comparison signals.

As to claim 11, figure 3 shows that the hysteresis arrangement further includes a hysteresis resistance (M6, M9); and the switch element includes a transistor (M62) that selectively removes the hysteresis resistance in response to a first state of the PUC signal and replaces the hysteresis resistance in response to a second state of the PUC signal.

As to claim 12, figure 3 shows that the transistor selectively shorts out the hysteresis resistance in response to the non-active state of the PUC signal, and enters a high impedance

state so as to replace the hysteresis resistance in response to the active state of the PUC signal, so as to adjust the second comparison signal.

Claims 13 and 15-20 recite similar limitations. Therefore, they are rejected for the same reasons.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 7, 8, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kureya et al. (JP 2003-283318).

As to claims 7 and 13; Kureya et al.'s figure 1 shows all limitations of the claims except for "a resistance ladder, operative with the p-channel MOSFET so as to provide the second comparison signal to the comparator". However, it is notoriously well known in the art that a resistor can be made by plurality of resistors connected in series in order to meet a desired resistance (R = R1 +R2 +... Rn). Therefore, it would have been obvious to one having ordinary skill in the art to use a resistor ladder for Kureya et al.'s R2 for the purpose of meeting a desired R2's resistance.

As to claim 8, the modified figure 1 shows that the second circuit is configured to provide the second comparison signal to that varies as a function of the supply voltage and crosses the first comparison signal when the supply voltage has increased to a value exceeding a sum of the first and second characteristic threshold voltages.

As to claim 14, figure 1 further shows a receiving circuit (3) that is configured and arranged to receive the PUC signal, that is connected to the same supply voltage as the PUC signal generating circuit. Figure 1 fails to show the detail of the receiving circuit. However, it is seen as an intended use for the receiver circuit including CMOS elements (NMOS and PMOS transistors).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Primary Examiner

June 30, 2005